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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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CHRISTIE, PARKER & HALE, LLP			TRAN, KHANH C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/640,963	Applicant(s) SHOHARA, AKI	
	Examiner Khanh Tran	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-20 is/are allowed.
- 6) ☒ Claim(s) 21-42, 44 and 45 is/are rejected.
- 7) ☒ Claim(s) 43 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08/16/2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The Amendment filed on 09/21/2005 has been entered. Claims 1-45 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 09/21/2005 have been fully considered but they are not persuasive. Examiner's responses to Applicant's arguments are incorporated to the claim rejection as shown below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 21, 26-27, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laskowski U.S. Patent 5,566,189.

Regarding claim 21, Laskowski invented a circuit and method for puncturing data on the transmission side of a digital communications system. In column 3, lines 29-67, figure 2 illustrates a puncturing circuit 18a including a

delay circuit 30, a multiplexer circuit 32, and a control circuit 42 implemented as a counter 44 and a decoder 46.

Laskowski does not expressly teach the claimed step of compressing a puncture mask. However, in column 2, lines 20-30, Laskowski further teaches the decoder, as part of the puncturing circuit 18a, is designed to decode a predetermined pattern and rate. The decoder can be further a programmable device, which would allow the desired puncture pattern and rate to be stored into the decoder.

In addressing Applicant's arguments on page 12 that claim 21, as amended, recites the step of compressing a puncture mask via a compression circuitry, which is not taught nor suggested by Laskowski teachings.

The Examiner responds that as discussed in the background of the invention in column 1 lines 30-45, Laskowski recognizes the shortfalls of prior methods of puncturing and depuncturing in which the entire puncture pattern is stored in shift registers. Because storing the entire puncture pattern in shift registers or similar components requires a relatively large amount of logic circuitry, particularly when the puncture pattern is long, Laskowski teachings stores the desired puncture pattern and rate in the decoder 46 of the puncturing logic circuit as shown in figure 2 in compressed form [Emphasis Added]. In column 3 lines 45-60, the decoder 46 decodes the desired puncturing pattern and rate to select which inputs (P1, P2, P1D, P2D) appear on the multiplexer

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outputs I, Q based on the puncturing pattern. In light of the foregoing disclosure, the decoder 46 equivalently decompresses the desired puncturing pattern.

Laskowski teaches storing the puncture pattern in compressed form, however, lacks the step of compressing a puncture pattern via a compression circuitry.

Nevertheless, because the decoder 46 can be programmed to store the compressed puncture pattern, one of ordinary skill in the art would have recognized that the punctured pattern would have been generated and compressed before being programmed into the decoder 46. In view of the foregoing discussion, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Laskowski teachings can be modified to use a logic synthesizer (part of the computer-aided design program) as suggested in Laskowski invention (see column 6 lines 10-20) to generate and compress the desired puncture pattern before programming to the decoder in the design phase. As further discussed in column 6 lines 10-20, the flexibility of the disclosed puncture circuit, along with its compatibility with computer-aided design, enables extremely fast re-designs, thus providing excellent reusability of the initial puncture circuit design.

As recited above, the decoder 46 can be further a programmable device, which would allow the desired puncture pattern and rate to be stored into the decoder. The decoder 46 is a conventional logic unit. Hence, the compressed

puncture pattern is stored electronically as claimed in the application claim. The puncture pattern corresponds to the claimed puncture mask.

In addressing Applicant's arguments on page 12 that Laskowski proposes a depuncturing circuit that is relatively simple and uses few logic components.

The Examiner responds that Laskowski proposes a puncturing [Emphasis added] logic circuit as shown in figure 2, not the depuncturing circuit as argued by Applicant. The desired puncture pattern in compressed form is stored or programmed into the decoder. The decoder decodes or decompresses the desired puncture pattern.

In further addressing Applicant's arguments on page 13 that Laskowski in fact teaches away from such a compression circuitry. The compression circuitry would increase the complexity of the decoder in that it would have to introduce a decompression circuitry to decompress the compressed pattern, which goes against Laskowski's goal of "a depuncturing circuit ...".

The Examiner responds that Laskowski teaches a puncturing logic circuit as shown in figure 2, not a depuncturing circuit as Applicant asserted in the Remarks. Laskowski puncturing logic circuit stores the desired puncture pattern and rate in compressed form. Laskowski does not teach the step of compressing the puncture pattern by a compression circuitry as claimed by Applicant. However, as recited above, because the decoder in the puncturing logic circuit

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stores the desired puncture pattern in compressed form, the desired puncture pattern is generated and compressed. For the foregoing reasons, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Laskowski teachings can be modified to use a logic synthesizer (part of the computer-aided design program) as suggested in Laskowski invention (see column 6 lines 10-20) to generate and compress the desired puncture pattern before programming to the decoder in the design phase.

Regarding claim 26, as recited above, the decoder 46 is a conventional logic unit. Hence, the compressed puncture pattern is stored electronically in a semiconductor memory.

Regarding claim 27, claim 27 is rejected on the same ground as for claim 21 because of similar scope.

Furthermore, Laskowski does not expressly teach the claimed step of retrieving a compressed puncture mask from a semiconductor. However, as recited in claim 21, Laskowski teaches the decoder 46, as part of the puncturing circuit 18a, is designed to decode a predetermined pattern and rate; see column 3, lines 45-60. The decoder 46 can be further a programmable device, which would allow *the desired puncture pattern and rate to be stored into the decoder*. Hence, in view of that, the decoder 46 retrieves and decodes the desired puncturing pattern and rate. Furthermore, the rejection argument in claim 21

addresses the claimed step of "the compressed puncture mask being generated according to a compression mechanism that compresses puncture mask data".

The decoder is designed to decode the predetermined puncture pattern; see column 2, lines 20-30. The foregoing teachings correspond to the claimed step of "decompressing the compressed puncture mask via a decompression circuitry". The decoder 46 corresponds to the claimed decompression circuitry.

The decoder controls the multiplexers 38, 40 and selects which inputs appear on I and Q according to the predetermined puncture pattern; see column 3, lines 35-45, and figure 2. The act of the decoder controlling the multiplexers addresses the claimed step of "deleting particular bits from a data sequence as set forth in the application claim".

Regarding claim 32, Laskowski does not expressly teach the claimed limitation "a bit in the decompressed puncture mask having a first polarity results in a first corresponding bit in the data sequence being deleted, and a bit in the decompressed puncture mask having a second polarity results in a second corresponding bit in the data sequence not being deleted". Laskowski discusses in the background of the invention that puncturing takes data out of the error corrected data stream in a predetermined puncture pattern applied at a predetermined puncture rate. As known in the art, a value of "0" in the puncture pattern indicates that the bit is to be deleted, and a value of "1" in the puncture pattern indicates that the bit is to be transmitted. In view

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of that a value of "0" in the puncture pattern corresponds to the first polarity and a value of "1" in the puncture pattern corresponds to the second polarity

Regarding claim 34, claim 34 is rejected on the same ground as for claim 27 because of similar scope. The claimed limitations "*each compressed puncture mask being generated via a compression circuitry that compresses puncture mask data*" has been addressed in claim 21. Furthermore, as recited in claim 27, also in column 2 lines 35-50, the puncturing circuit is easily designed for a variety of puncture patterns and rates using computer-aided circuit. The puncture pattern and rate can be easily changed by simply redesigning and replacing the decoder. Laskowski does not expressly teach the puncture circuit in figure 2 stores a plurality of compressed masks. Nevertheless, because decoder 46 can store compressed puncture pattern, one of ordinary skill in the art at the time of the invention would have been motivated to store a plurality of puncture patterns. Motivation is to have more flexibility on the rate by varying different puncture patterns. As recited in claim 27, the decoder 46 retrieves and decodes the compressed puncturing pattern and rate. Hence, the decoder 46 corresponds to the claimed decompression circuitry.

4. Claims 22-25, 28-31, 35-39, 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laskowski U.S. Patent 5,566,189 as applied to claims 21 and 34 above, and further in view of Li U.S. Patent 6,385,752 B1.

Regarding claims 22 and 28, Laskowski does not teach employing puncture pattern of any particular length.

Li invention is directed to an improved method of puncturing a convolutionally encoded bit stream provided for specific examples consisting of PCS-4 and PCS-5, these being encoding schemes provided in accordance with the EDGE standard. For PCS-5 in one case, the blocks to be punctured have a size of $L=2422$, and said blocks need to be punctured such that $M=1384$ bits remain. In view of that the length of the puncture mask is more than 1000 bits. Laskowski invention differs from Li invention in that Laskowski teachings do not disclose any particular length of the puncture pattern. However, Laskowski expresses that the puncture circuit is easily designed for a variety of puncture patterns; see column 2, lines 35-45. Furthermore, Laskowski recognizes that storing the entire puncture pattern in shift registers or similar components requires relatively large amount of logic circuitry, particularly when the puncture pattern is long. In view of the foregoing discussion, it would have been obvious for one of ordinary skill in the art at the time of the invention that Laskowski puncture circuit can be modified to accommodate long puncture patterns, e.g. more than 1000 bits, as taught in Li invention.

Regarding claims 23, 29 and 36-37, claims 23, 29 and 36-37 are rejected on the same ground as for claim 22 because of similar scope.

Regarding claims 24, 30 and 38, Li invention applies to encoding schemes in accordance with existing EDGE standards for PCS-4 and PCS-5.

Regarding claims 25, 31 and 39, as taught in column 2, lines 20-50, see also figure 2, the decoder 46 can be programmable device, which would allow the desired puncture pattern and rate to be stored or programmed into the decoder 46.

Furthermore, the puncture circuit is designed for a variety of puncture patterns and rates. In view of that, storing at least 30 puncture masks would have been apparent to one of ordinary skill in the art.

Regarding claim 35, Laskowski does not teach the puncture circuit further comprising circuitry for wireless communications. Nevertheless, as well known in the art, puncture circuit is utilized on the transmission circuit to reduce the data rate due to error correction that increases bandwidth requirements of the transmission medium. In view of the foregoing, it would have been obvious for one of ordinary skill in the art at the time of the invention Laskowski puncture circuit can be implemented into Li transmitter as shown in figure 1, the transmitter in figure 1 being wireless communication transmitter.

Regarding claim 40, the communication system in figure 1 of Li invention includes a receiver 14 wherein the receiver 14 comprises known components, such as a mixer in the down-converting section as appreciated by one of ordinary skill in the art, see column 3, lines 20-35 of Li invention.

Regarding claims 41-42, the communication system in figure 1 of Li invention includes a transmitter 12 wherein the transmitter 12 comprises general components, such as a mixer in the up-converting section, a VCO as appreciated by one of ordinary skill in the art, see column 3, lines 1-16 of Li invention.

5. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Laskowski U.S. Patent 5,566,189 as applied to claim 27 above, and further in view of admitted prior art in the original disclosure and Laskowski U.S. Patent 5,790,566.

Regarding claim 33,

Laskowski discloses in another US Patent '566' a method for de-puncturing data in a receiver. As known in the art, the de-puncturing process is the reverse of the puncturing process, in which puncture patterns are known to the receiver. Similar to US Patent '189', in column 1, lines 20-35, Laskowski discusses problems in prior methods in which storing the entire puncture pattern in shift registers or similar components requires a relatively large amount of logic circuitry, particularly when the puncture pattern is long. In light of the foregoing problem, in column 2, lines 10-25, see also figure 2, the decoder can be a programmable device, which would allow the desired pattern and rate to be stored or programmed into the decoder. Using similar argument as discussed in claim 21, the desired pattern is compressed and stored in the memory of the decoder. Also, in column 2, lines 10-25, the decoder in figure 2 is designed to decode the predetermined pattern sequence. Therefore, referring to figure 2,

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- data are read in serially on I and Q path,
- as recited above, the decoder in figure 2 is designed to decode the predetermined sequence one bit at a time according to counter 44, which keeps track of the number of positions in the puncture pattern and rate and communicates to the decoder 46 the current position of the de-puncture pattern.
- Laskowski, however, does not disclose inserting an erasure and not inserting an erasure as set forth in the instant application. Admitted prior art discloses on page 2 of the original disclosure that a zero indicates a position where an erasure is to be inserted, which corresponds to a first polarity, and a one indicates a position where an erasure is not to be inserted, which corresponds to a second polarity. Since utilizing an erasure is well known in the art, therefore, it would have been obvious for one of ordinary skill in the art to modify Laskowski teachings for depuncturing data in the receiver circuitry can be modified to implement in such a way that a zero indicates a position where an erasure is to be inserted and a one indicates a position where an erasure is not to be inserted as taught in prior art.

6. Claims 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laskowski U.S. Patent 5,566,189 as applied to claim 21 above, and further in view of Abe et al. U.S. Patent 6,693,889 B1.

Regarding claim 44, Laskowski does not teach the claimed step of generating an intermediate puncture mask based on the puncture mask.

Abe et al. discloses a multiple puncturing pattern generator as shown in figure 2A. In column 7 line 55 via column 8 line 20, a matrix converter 202 outputs a plurality of puncturing patterns by converting a row, a column or matrix elements of the reference matrix 201a according to a predetermined process. Abe et al. further teaches the system is able to save a memory capacity by storing only one matrix as a reference to generate a plurality of puncturing patterns. Laskowski and Abe et al. inventions are in the same field of endeavor, and both teachings are designed not to store long puncture patterns to save memory. Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that Laskowski puncture circuit can be modified to include Abe et al. teachings. In view of that the reference matrix can be compressed and stored in the decoder as shown in figure 2 of Laskowski invention. Furthermore, reference matrix generator 201 generates a reference matrix according to a predetermined pattern matrix.

Regarding claim 45, with the combining teachings as discussed in claim 44, the decoder 46 of Laskowski invention decodes the reference matrix, which is used to output one of the puncturing patterns.

Allowable Subject Matter

7. Claims 1-7 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, claim is directed to a method of compressing puncture mask information. Claim is allowable over prior art of record because the cited references, either singularly or in combination, cannot teach or suggest the claimed method as set forth in the claim.

8. Claims 8-18 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, claim is directed to a method of decompressing and using a puncture mask. Claim is allowed over prior art of record because the cited references, either singularly or in combination, cannot teach or suggest the claimed method as set forth in the claim.

9. Claims 19-20 are allowed.

Regarding claim 19, claim is directed to a code puncture apparatus. Claim is allowed over prior art of record because the cited references, either singularly or in combination, cannot teach or suggest the claimed code puncture apparatus comprising a run length decoder, a differential operator, and a puncture mask register as set forth in the claim.

10. Claim 43 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-

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3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Pham Cong Tran 12/09/2005

Examiner KHANH TRAN